APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/918,380	07/30/2001	Indra Laksono	VIXS.0100090	9961

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EXAMINER
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ART UNIT	PAPER NUMBER
2621	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
Office Action Summary	09/918,380	LAKSONO ET AL.
	Examiner	Art Unit
	Nhon T. Diep	2621

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _____.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *13-29,31-40,43-50,52 and 53* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *13-29,31-40,43-50,52 and 53* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *7/30/2001* is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the
United States before the invention thereof by the applicant for patent, or on an international application
by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this
title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act

of 1999 (AIPA) and the Intellectual Property and High Technology Technical

Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior

to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2.   Claims 13-29, 31-35, 37-40, 43-50, 52-53 are rejected under 35 U.S.C. 102(e) as

being anticipated by Eifrig et al (cited by the applicants).

Eifrig et al discloses a transcoder-multiplexer architecture comprising the same

integrated single chip system comprising: a first processor to receive digital video data

and provide parsed video data (fig. 1a, el. 10); a second processor coupled to the first

processor to access the parsed video data, the second processor including a video

transcoder (fig. 1a, el. 30, notice that preamble recites an integrated single chip,

however, the preamble is not referred to in the body of the claim) as specified in claim

13; wherein the first processor is a general purpose processor (fig. 1a, el. 10) as

specified in claim 14; wherein the second processor further includes: a data

decompression portion; a scalar; and a data compression portion (col. 4, ln. 11-25) as

specified in claim 15; wherein the decompression portion includes a portion to perform a

frequency domain to time domain transform (IDCT) as specified in claim 16; wherein the

frequency domain to time domain transform portion is a portion to perform an inverse

discrete cosine transform portion as specified in claim 17; wherein the decompression

portion includes a portion to perform a de-quantization of data (IQ) as specified in claim

18; wherein the decompression portion includes a portion to perform a DeZigZag of

data (VLD) as specified in claim 19; wherein the decompression portion includes a

motion compensation portion (fig. 6, el. 620) as specified in claim 20; wherein the

decompression portion includes a motion compensation portion (fig. 6, el. 620) as

specified in claim 21; wherein the decompression portion includes a motion

compensation portion (fig. 6, el. 620) as specified in claim 22; wherein the compression

portion includes a motion vector generator (MV as inputted to el. 620) as specified in

claim 23; wherein the motion vector generator includes a buffered motion predictor (el.

630, 640) as specified in claim 24; wherein the compression portion further includes a

portion to perform a time domain to frequency domain transform (col. 4, ln. 17) as

specified in claim 25; wherein the time domain to frequency domain transform portion

includes a discrete cosine transform portion (col. 4, ln. 17) as specified in claim 26;

wherein the compression portion includes a motion vector generator (MV as inputted to

el. 620) as specified in claim 27; wherein the motion vector generator includes a

buffered motion predictor (el. 630, 640) as specified in claim 28; wherein the second

processor is coupled to the first processor through a memory controller and a

sequencer (el. 10 and 20) as specified in claim 29; a method comprising: receiving, at a

first processor, a data stream including video data; parsing, at the first processor, the

data stream to identify video data associated with a first channel (fig. 1a, el. 10);

packetizing, at the first processor, the video data associated with the first channel to

generate the one or more packets, each packet having a video data payload and

information related to the video data payload, wherein the video data payloads of the

one or more packets represent a first channel of compressed video data having a

characteristic represented by a first value (output to el. 20); receiving, at a second

processor, the one or more packets; and transcoding, at the second processor, the

video data payloads of the one or more packets to generate a representation of a

second channel of compressed video data having the characteristic represented by a

second value (fig. 1a, el. 30) as specified in claims 44 and 53; wherein the characteristic

is a compression factor (fig. 6, el. 650) as specified in claims 31-32 and 45-46; wherein

transcoding the video data payloads comprises: decompressing the video data

payloads to generate a first intermediate data; scaling the first intermediate data to

generate a second intermediate data; and compressing the second intermediate data to

generate the representation of the second channel (fig. 1a, el. 30 and fig. 6) as specified

in claim 33; wherein transcoding the video data payloads comprises: decompressing the

video data payloads to generate a first intermediate data, wherein the first intermediate

data is frequency domain data; converting the first intermediate data to a second

intermediate data, wherein the second intermediate data is time domain data having the

characteristic represented by the first value; converting the second intermediate data to

a third intermediate data having the characteristic represented by the second value; and

compressing the third intermediate data to generate the representation of the second

channel (figs. 6, 7, 8) as specified in claim 34; wherein receiving the one or more

packets includes: storing the video data payloads of the one or more packets in a first

memory of the second processor; and storing the information associated with the video

data payloads in a second memory of the second processor (fig. 6, el. 630, 640) as

specified in claim 35; wherein the video data payloads are transcoded based at least in

part on the information associated with the video data payloads (MV-620-615-A1-Q2) as

specified in claim 37; wherein the information associated with a video data payload

indicates that the video data payload includes one or more of video time stamp

information, picture configuration information, slice information, macroblock information,

motion vector information, quantizer matrix information, or specific picture location

information (MV) as specified in claim 38; wherein receiving the one or more packets

and transcoding the video data payloads support a real-time play back of the

representation of the second channel (col. 23, ln. 64 – col. 24, ln. 7) as specified in

claim 39; further comprising: providing the representation of the second channel of

compressed video data for reception by at least one multimedia device (fig. 1a, output

of el. 40) as specified in claim 40; wherein the first data processor includes a general

purpose processor and the second data processor includes a video processor (el. 10,

30) as specified in claim 43; wherein the first data processor is further to: decompress

the video data payloads to generate a first intermediate data (fig. 1a, el. 20); scale the

first intermediate data to generate a second intermediate data (fig. 6, el. Q2); and compress the second intermediate data to generate the representation of the second channel (fig. 6, el. 680) as specified in claim 47; wherein the first processor is further to: decompress the video data payloads to generate a first intermediate data, wherein the first intermediate data is frequency domain data; convert the first intermediate data to a second intermediate data, wherein the second intermediate data is time domain data having the characteristic represented by the first value; convert the second intermediate data to a third intermediate data having the characteristic represented by the second value; and compress the third intermediate data to generate the representation of the second channel (fig. 6, DCT, IDCT, Q1, Q2) as specified in claim 48; wherein the first processor transcodes the video data payloads based at least in part on the information associated with the video data payloads (MV) as specified in claim 49; wherein the information associated with a video data payload indicates that the video data payload includes one or more of video time stamp information, picture configuration information, slice information, macroblock information, motion vector information, quantizer matrix information, or specific picture location information (MV) as specified in claim 50; wherein the first data processor comprises a video processor and the second data processor comprises a general purpose processor (fig. 1a, el. 10. 30) as specified in claim 52;

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eifrig et al.

As applied to claim 35 above, it is noted that Eifrig et al does not particularly disclose that the buffer memories as used to hold video data payloads and associated video information are the same type of buffer memory nor they are of the different type of memory; however, in the absence of any contradictory teachings, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to construct the first memory and the second memory as of the same type of memory for the sake of simplicity.

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Iwata (US 6,172,621 B1) discloses a high speed coding apparatus using parallel processing system.

b. van Hook et al (US 6,567,426 B1) discloses a preemptive timer multiplexed shared memory access, wherein multiple processors and data memory are all disposed on a single integrated chip (IC).

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhon T. Diep whose telephone number is 571-272-7328. The examiner can normally be reached on m-f.

   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ND
2/3/2007   **NHON DIEP**
                                                            PRIMARY EXAMINER